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REMARKS

Entry of this Amendment and reconsideration are resp ctfully requested in view of the amendments made to the claims and for the remarks mac herein.

Claims 1-7, 9-13 and 15 are pending in the application id stand rejected.

Claim 1 has been amended.

Claims 1-7, 9-13 and 15 stand rejected under 3: USC §103(a) as being unpatentable over Sindhu (USP no. 5,440,698) in view of Fost (USP no. 6,202,007) and further in view of Denneau (USPPA 2003/00287247).

Applicant respectfully disagrees with and explicitly traverses the reason for rejecting the claims. However, in order to advance the p osecution of this matter, independent claim 1 has been amended to further recite the subject matter claimed in better form and to explicitly recite that at least one local emory unit is selectively accessed according to an address range and that the at lea one local memory units corresponding to selected processors. No new matter has be n added. Support for the amendment may be found at least on page 9, lines 29-33 ("a l data processing units IP are able to access the off-chip memory SDRAM and a fur er on-chip local memory MEM attached to the memory interface MMI, but not all data rocessing units IP are able to access all on-chip local memories MEM attached to the hul H_{11}, H_{12} and H_{2}.").

Sindhu (USP no. 5,440,698) discloses an arbitra on system for resolving contention on synchronous packet switched busses to ensure iat all devices serviced by such a bus are given bounded time access to the bus and to p mit such devices to fill all available bus cycles with packets. Flow control for shared emory is implemented by supporting different types of arbitration requests and priori ation of such requests by type. Sindu fails to provide any teaching regarding a sing : memory space or using memory addresses to distinguish between local and global me iory.

Foster (USP no. 6, 202,097) discloses a method or performing diagnostic functions in a multiprocessor data processing system. Foster cited by the Office Action for teaching a communication interface positioned on a singl chip, wherein the memory device is not positioned on the single chip.

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Denneau (USPPA no. 2003/0028747) discloses a flexi e method for associating cache memories with processors and a main memory whe ein an effective address comprises an interest group and an associated address. The i erest group represents an index into a cache vector table and/or an entry into the cache v tor table. The associated address is used to select one of the caches. In one aspect, onl the interest group may be used to represent an address used for access.

The Office Action refers to col. 5, lines 20-23 of Sindl for teaching a cache-like hierarchy, and col. 16, lines 44-52 for teaching shared write pdating "which implies a shared address space." The Office Action further refers to cc 22, line 41- col. 23, line 27 for teaching that when data is not found in lower mer ory, a higher memory is checked and then the lower level is updated. The Office Ac on concludes that Sindhu implicitly teaches a shared memory similar to that recited in th claims.

However, a review of the referred to section reveals th : Sindu discloses a system wherein the memory is organized with different bit settings t determine the position of data in the cache memories and global memory. See, for e: mple, col. 23, lines 1-54, which state, "[w]henever the second-level cache 19a receives RBRqst from a resquestor on its cluster bus 15a, the second-level cache 19a may or ma not contain a copy of the data block specified by the RBRqst. If it has a copy, the sec nd-level cache returns the data to the requestor ... after setting the reply Shared bit the reply packet to the logically ORed SharedIn value of (a) the SharedOut signals t it it receives from the first level caches as a result of the RBRqst and (b) the current st e of its shared bit for the specified data block ... If, on the other hand, the second-leve cache 19a does not have a copy of the data block that is specified by the RBRqst ... ie second-level cache 19a issues a RBRqst packet on the global bus... When a seconc evel cache, such as cache 19a, receives a WSRqst from a requestor on its cluster bu the cache 19a checks to determine if its shared bit for the data block containing tl address specified by the WSRqst is set. If its shared bit for that particular data block is not set, the second level cache 19a updates the data in accordance with the WSRqs sets its owner bit for the updated block and then issues a WSRply ... via its cluster bus ..."

Hence, Sinhdu teaches that a check for a copy of the ata is made in the memory and if a copy is not available in the local memory (cache) th a next level of memory is

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checked. However, Sinhdu fails to disclose that the globa and local memories are organized such that an address range defines the particular iemory. Rather Sindhu performs checks on the data content to determine whether the ta is in a lower level and dependent upon the shared bit setting performs additional pr essing in a higher level memory. Sindu is completely silent with regard to the a dressing of each of the memories. And it cannot be implied or considered inhe nt that the memory is designated over a single memory space.

Foster fails to provide any teaching regarding the e of address ranges for distinguishing global and local memories as is recited in the cl ns.

Denneau teaches that a range of addresses may be use to define particular cache memory wherein a first range defines a first cache memory iat is accessed by a first processor and a second, disjoint, range defines a second cacl memory that is accessed by a second processor. Denneau further defines a third, d joint, range that may be accessed by both the first and second processor (see Figure 3 Thus, Denneau teaches a system wherein a single main memory is divided into a plur ity of ranges that may be accessed by processors based on the settings of one or more ac ess bits.

However, the combination of the cited references fail: o teach a memory device and at least one local memory units sharing a single address pace where local memory units are associated with, and accessed by, corresponding pr essors, as is recited in the claims.

In order to establish a *prima facie* case of obviousness hree basic criteria must be met, 1. there must be some suggestion or motivation, either i the references themselves or in the knowledge generally available to one of ordinary sl ll in the art, to modify the reference or combine the reference teachings, 2. there must a reasonable expectation of success; and 3. the prior art reference must teach or sugges ll the claim limitations.

In this case, a *prima facie* case of obviousness has n been made as each of the elements recited in the claims is not disclosed by the combi tion of Sindhu, Foster and Denneau.

For the amendments made to the independent claim and for the remarks made herein, applicant submits that the rejection of the independen claim 1 has been overcome and respectfully requests that the rejection be withdrawn.

With regard to the remaining claims, these claims depe . from independent claim 1, which has been shown to include subject matter not disclo d by the combination of Sindhu, Foster and Denneau. Consequently, the remaining dep ident claims are also not rendered obvious by Sindhu, Foster and Denneau as the remai ig dependent claims also include subject matter not disclosed by the cited references.

For the amendments made to the claims and for t e remarks made herein, applicant submits that all the objections and rejections have b n overcome and that the claims are in a condition for allowance. Applicant respectfull requests that a Notice of Allowance be issued.

Should the Examiner believe that the disposition of a / issues arising from this response may be best resolved by a telephone call, the Exa iner is invited to contact applicant's representative at the telephone number listed below

Respectfu / submitted,
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